|  |  |
| --- | --- |
| Name: Abdullah Nadeem Waraich | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-126 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual 4**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

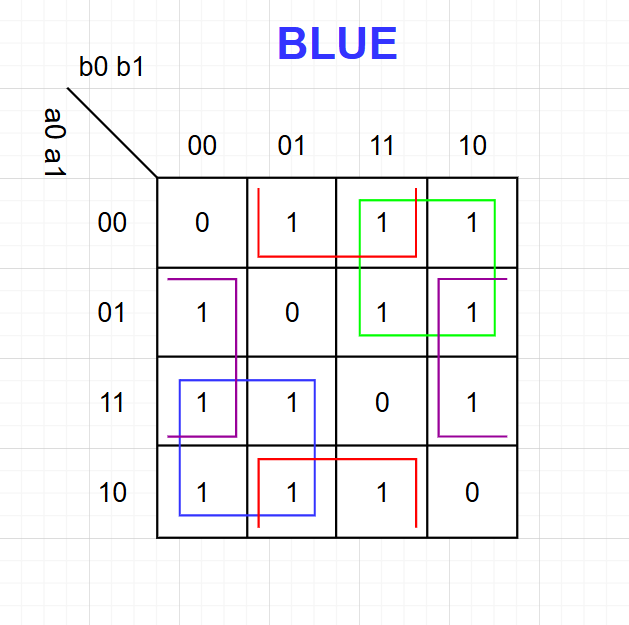
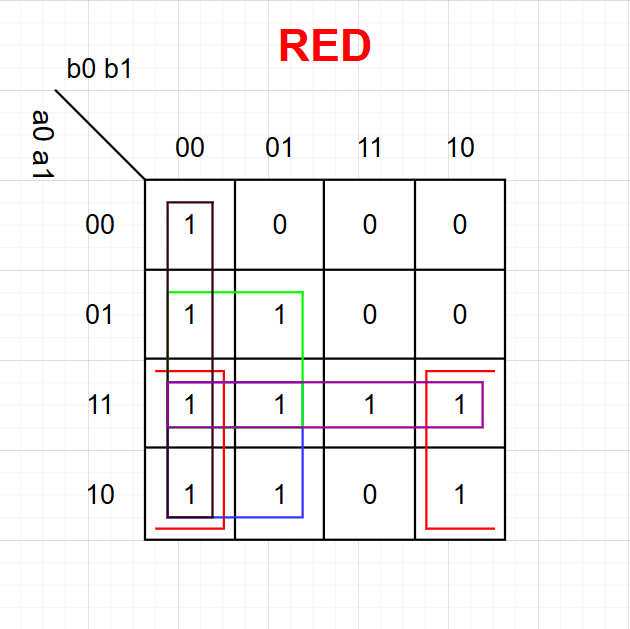
**PART 1:**

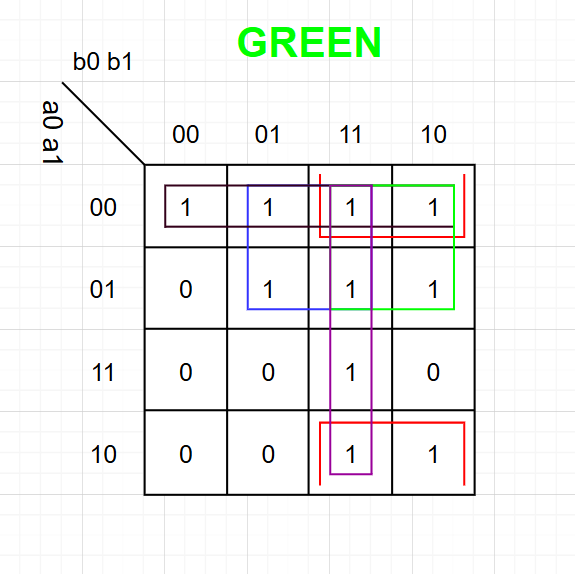
**Results and Findings:**

1. Truth table of circuit:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | **Outputs** | | |
| **a** | **b** | **Red** | **Green** | **Blue** |
| 00 | 00 | 1 | 1 | 0 |
| 00 | 01 | 0 | 1 | 1 |
| 00 | 10 | 0 | 1 | 1 |
| 00 | 11 | 0 | 1 | 1 |
| 01 | 00 | 1 | 0 | 1 |
| 01 | 01 | 1 | 1 | 0 |
| 01 | 10 | 0 | 1 | 1 |
| 01 | 11 | 0 | 1 | 1 |
| 10 | 00 | 1 | 0 | 1 |
| 10 | 01 | 1 | 0 | 1 |
| 10 | 10 | 1 | 1 | 0 |
| 10 | 11 | 0 | 1 | 1 |
| 11 | 00 | 1 | 0 | 1 |
| 11 | 01 | 1 | 0 | 1 |
| 11 | 10 | 1 | 0 | 1 |
| 11 | 11 | 1 | 1 | 0 |

(b)





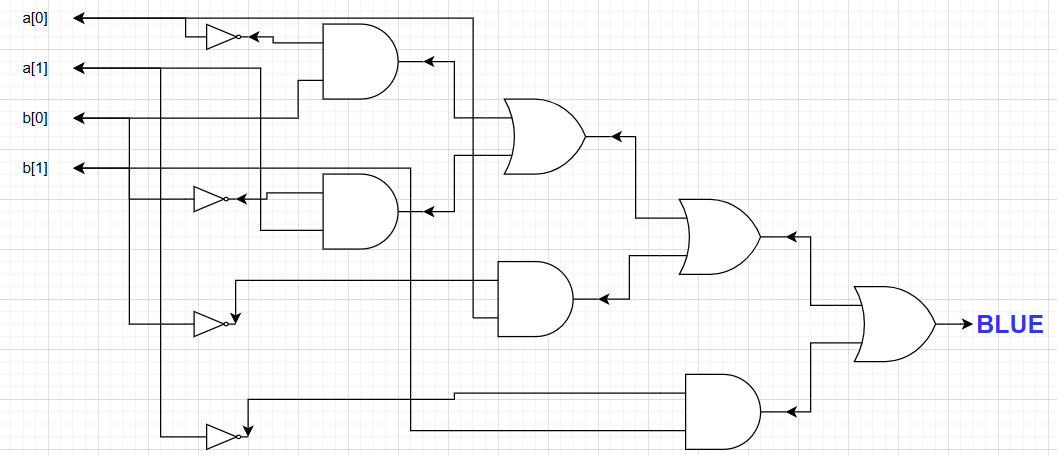
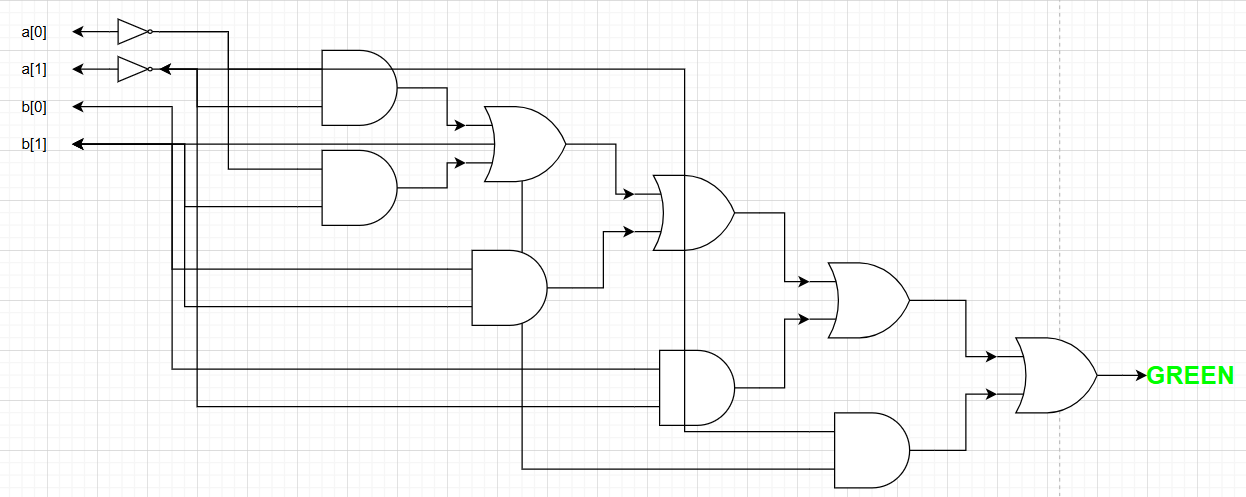
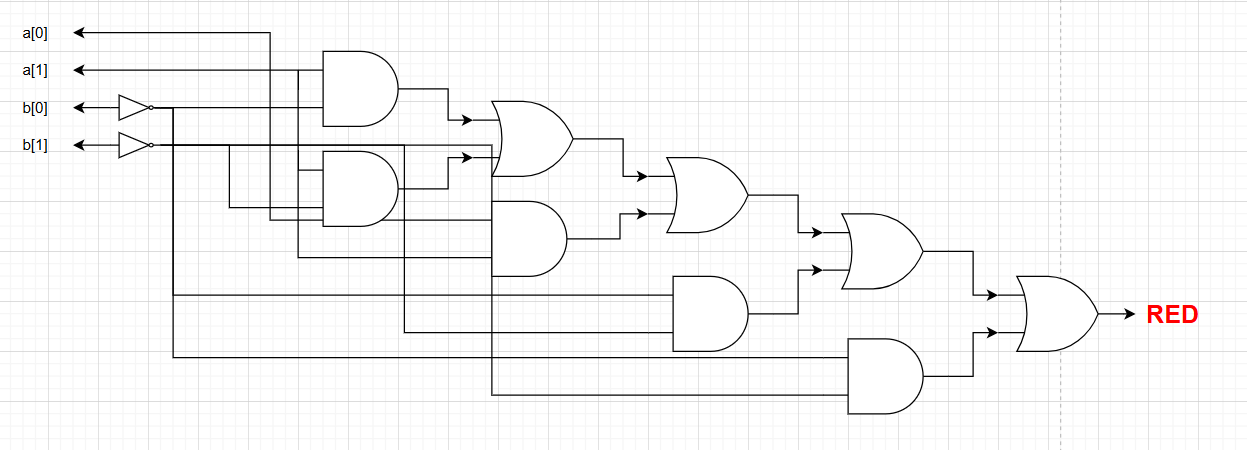
Equations Created Using Essential Prime Implicants

**red = (a1 .~b0) + (a1 .~b1) + (a0 . a1) + (~b0 .~b1) + (a0.~b1)**

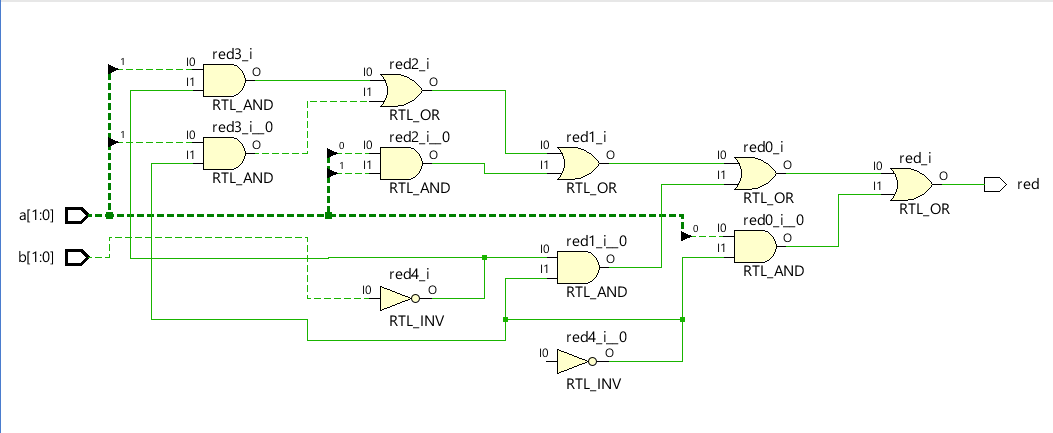
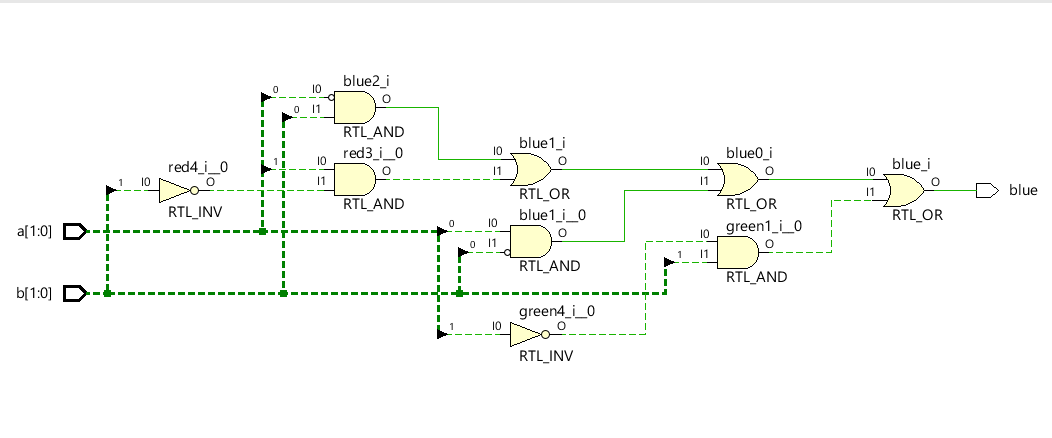
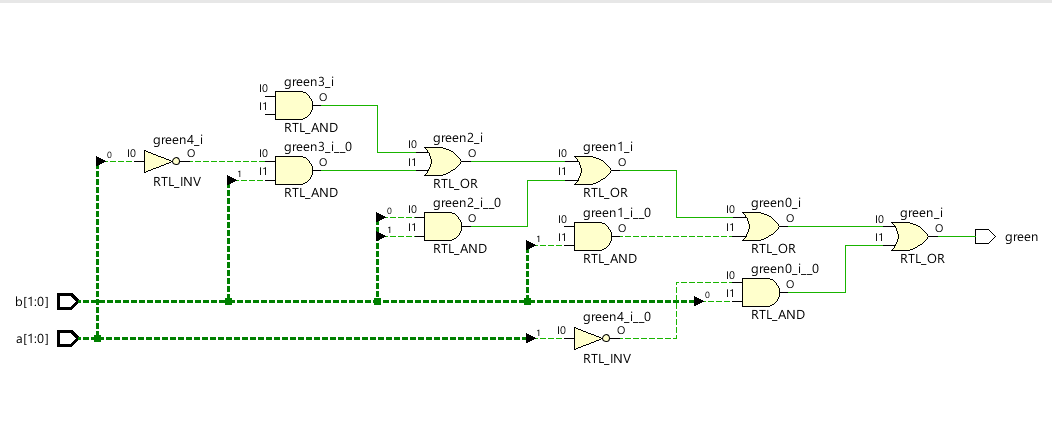
**blue = (~a0 . b0) + (a1 . ~b1) + (a0 . ~b0) + (~a1 . b1)**

**green = (~a0 . ~a1) + (~a0 . b1) + (b0 . b1) + (~a1 . b1) + (~a1 . b0)**

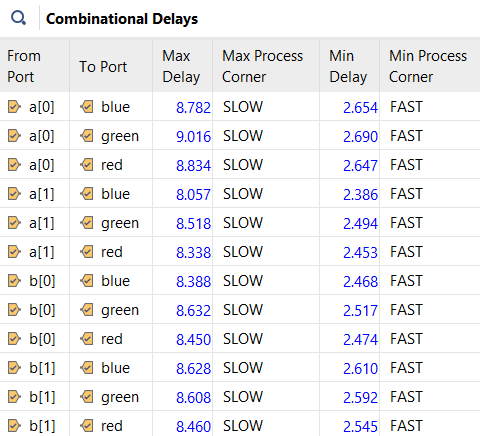
(c)

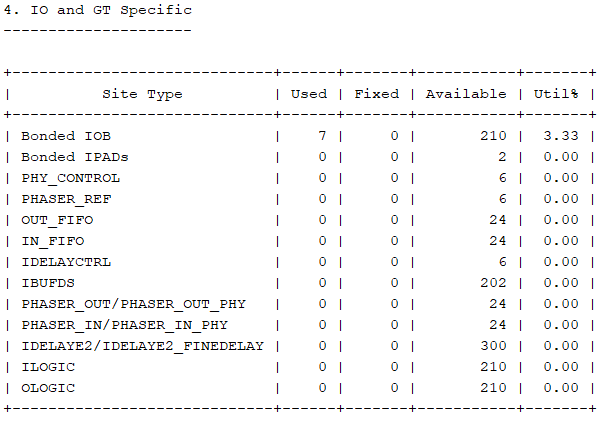
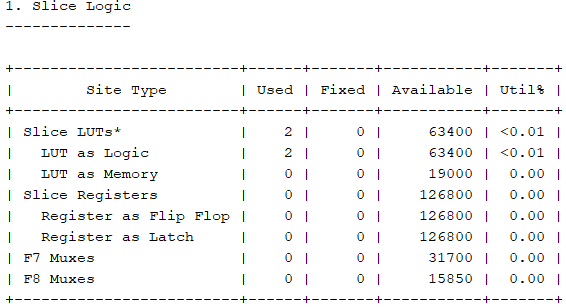
(d) The Schematics By Vivado and The Circuits Made by K-Maps are the same.

(e) The Maximum Combinational Delay is from a[0] to green which is 9.106.



(f) The Number of LUTs used is 2 and The Number of IOs Port used is 7.



**PART 2:**

System Verilog Code:

**`timescale 1ns / 1ps**

**module tricolor(**

**input logic [1:0] a,**

**input logic [1:0] b,**

**output logic red,green,blue**

**);**

**assign red = (a[1] & ~b[0]) | (a[1] & ~b[1]) | (a[0] & a[1]) | (~b[0] & ~b[1]) | (a[0] & ~b[1]);**

**assign blue = (~a[0] & b[0]) | (a[1] & ~b[1]) | (a[0] & ~b[0]) | (~a[1] & b[1]);**

**assign green = (~a[0] & ~a[1]) | (~a[0] & b[1]) | (b[0] & b[1]) | (~a[1] & b[1]) | (~a[1] & b[0]);**

**endmodule**